## REMARKS

The claims have been amended in view of the Office action and in view of the remarks which follow, they are believed to be in condition for allowance. Claims 4 and 11 have been replaced by new claims 21 and 22 in view of the Drawings objection discussed below. The claims have been narrowed to cover the fact that nitridation of the PFET dielectric layer has produced a first optimized concentration level of nitrogen atoms in the PFET dielectric layer and the nitridation of the NFET dielectric layer has been produced a second optimized concentration level of nitrogen atoms in the NFET dielectric layer. Claim 9 and claims dependent thereon are now believed to be patentable since they contain limitations taken from claim 10 which was not rejected over the prior art and which is assumed to be allowable as claim 10 has been amended to overcome the 35 U.S.C. § 112 grounds of rejection asserted against it in the Office Action. The added language in claim 9 reads as follows:

> "forming a PFET mask over said PFET area prior to beginning nitridation of said NFET gate oxide layer, then performing NFET gate dielectric nitridation of said NFET gate oxide layer to form said NFET gate dielectric layer above said NFET area producing a second optimized concentration level of nitrogen atoms in said NFET gate dielectric layer above said NFET area and then removing said PFET mask,".

Claim 20 is believed to be patentable because it has been amended to include the subparagraphs reading as follows:

> "said PFET gate dielectric layer above said PFET area being nitrided with a first optimized concentration level of nitrogen atoms in said PFET gate dielectric layer above said PFET area,
>
> said NFET gate dielectric layer above said NFET area being nitrided with a second optimized concentration level of nitrogen atoms in said NFET gate dielectric layer above said NFET area,"

As will be pointed out below, claim 20 covers a new and unobvious structure which is believed to be unobvious over the prior art of record.

## Drawings

In the Detailed Action, an objection was raised to the drawings under 37 CFR 1.83(a) with respect to claims 4 and 11. The Office Action stated that the objectionable "features must be shown or the features canceled from the claims 4 and 11. No new matter should be entered." Claims 4 and 11 were canceled and new claims 21 and 22 include different language which is

believed to render the grounds of rejection moot, since the language which had been used in claims 4 and 11 has been replaced with language based upon FIGS. 7A-7D of the drawings.

Objection To Specification

The Office action stated as follows:

> "The specification is objected under 37 CFR 1.75(d) as failing to disclose an equal concentration of nitrogen in NFET and PFET areas. Appropriate correction is required."

Claim 3 and 10 have been amended to make it clear that what is involved is providing an "additional" concentration of nitrogen in the NFET and PFET areas, as shown in FIGS. 6A-6D. The word "equal", while technically correct in that the plasma 19N' is applied equally to both areas in FIG. 6C, the language used in the specification is "additional", so that word is appropriate, in the context of the teachings of the specification and drawings. Thus, in view of the amendments to claims 3 and 10 the issue is now believed to be moot.

Claim Rejections - 35 U.S.C. § 112

Claims 3, 7, 10 and 15 were rejected under 35 U. S . C. 112, second paragraph. The Office Action stated as follows:

> "In claim 1, the nitrogen concentration in PFET and NFET gate oxide areas are different and in claims 3 and 10 the nitrogen concentration in PFET and NFET oxide areas are the same. Therefore a non-sequitor [sic] exists."

The word "equal" previously appeared in claims 3 and 10 which have been amended as stated above to render this issue moot by substituting the word "additional" for "equal."

Claims 7 and 15 were rejected as being dependent upon indefinite claim. Claim 3 upon which claims 7 and 15 are dependent have been amended, so the alleged indefiniteness is believed to have been overcome.

Claims 3 and 10 were rejected for the reciting the limitation "the other of said regions" in claim 3, line 4 and claim 10, line 12 on the basis that there was " insufficient antecedent basis for this limitation in the claim." The claims have been amended to remove this ground of rejection by referring to appropriate antecedents. Accordingly this ground of rejection is also believed to be moot now.

Claim Rejections - 35 U.S.C. § 103

Claims 1, 5, 9, 12 and 20 were rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Trivedi et al. (U. S. Patent 6,541,395) hereinafter Trivedi '395.

The Office Action stated as follows:

"Regarding claims 1, 5,9, 12 and 20 Trivedi et al disclose the following:

"In column 3 lines 24-63, and figure 1- 7 a method of forming CMOS semiconductor materials with a PFET area (12) and a NFET area (14) formed on a semiconductor substrate (10)."

"In column 2 and lines 20-21, 29-30 and lines 45-52, a PFET gate dielectric (28) and a NFET gate dielectric (32) composed of silicon oxide with different degrees of nitridation."

"In column 5 lines 4l-44, Trivedi et al also disclose that NFET gate dielectric layer and PFET gate dielectric layer can have same thickness."

"Trivedi et al. do not disclose specifica1y nitridation of NFET gate dielectric. However in column 5 and lines 36-37, Trivedi et al. disclose that NFET gate dielectric with nitrogen concentration less than or equal to 0.1% molar and in column 2 and lines 48-50, PFET gate dielectric with nitrogen concentration of 0.1% molar to 10% molar. Therefore nitridation occurring in some form on NFET gate dielectric is at least suggested in Trivedi et al. Trivedi et al. also disclose that nitrogen concentration in PFET gate dielectric and in NFET gate dielectric are different and nitrogen concentration in PFET gate oxide layer is higher than that of NFET gate oxide layer."

"It would have been obvious to one having an ordinary skill in the art at the time the invention was made to incorporate teachings of Trivedi et al. in forming a semiconductor device with NFET and PFET devices with the object of optimizing the electrical properties of thin gate dielectrics of PFET and NFET devices."

The claims have been amended to make it clearer that the gate oxide layers of the NFET and PFET devices of the instant invention have been tuned to different optimized levels of nitridization which is a concept which is not suggested by Trivedi '395, which teaches nitridization of only the first dielectric layer 28 with nitrogen source 50 in FIG. 3 and then subsequently forming a second dielectric layer 32 which is substantially void of nitrogen. Thus the "plain meaning" of Trivedi '395 is that only one the layer 28 has nitrogen added into its composition and that inadvertently only a trace of nitrogen might be present in layer 32. There is no suggestion shown in Trivedi '395 for providing optimized levels of nitridation in layer 32 of, which states in the Abstract as follows:

"The second gate dielectric layer is a silicon dioxide material substantially void of nitrogen atoms." [Emphasis added]

<u>Rejection is Based on Forbidden Hindsight</u>

In view of that the above statement in the Abstract, it is respectfully submitted that the Office Action makes a very human mistake of using impermissible hindsight in arguing that the presence of a trace amount of nitrogen in the NFET gate dielectric layer 32 of Trivedi '395

suggests providing an optimized level of nitrogen therein. It is a fact that the gate dielectric layer 32 is ***substantially***, i.e. nearly completely, ***void of nitrogen***. That is not believed to make the process of optimization of as claimed in the amended claim 1 of "providing nitridation of said NFET gate oxide layer to form said NFET gate dielectric layer above said NFET area with a second optimized concentration level of nitrogen atoms in said NFET gate dielectric layer above said NFET area,". There is no suggestion of providing nitridation of the layer 32 of Trivedi '395. Thus it is believed that claim 1 and claims dependent thereon are clearly patentable over the prior art of record.

Trivedi '395 Did Not Contemplate the Problem Solved by the Instant Invention.

The present application deals with the problem of gate leakage reduction and mobility in the NFET devices. In the background of the present invention, it is stated as follows:

> "Nitrogen in NFET is beneficial for gate leakage reduction, but degrades mobility when the N concentration is too high."
>
> "Nitrogen in PFET reduces gate leakage / boron penetration, improves mobility."
>
> "The combination of the previous two facts (which is not generally known) leads one to want to optimize PFET and NFET gate oxide separately."

The problem of how to provide a device which has excellent leakage reduction and adequate mobility is not addressed by Trivedi '395. Thus the reference fails to suggest the method and device claimed herein.

Trivedi '395 Teaches Away from Providing Nitrogen in the NFET Gate

It is respectfully submitted that Trivedi '395., in fact, actually "teaches away" from the invention claimed herein rather than encouraging persons of ordinary to take the path applicants took in addressing the problem solved by the instant invention. It is believed to be clear that Trivedi '395 intended to provide a second gate dielectric layer of silicon oxide with nothing more than a trace of nitrogen. The statements about "substantially void of nitrogen atoms" manifest the difficulty in avoiding inclusion of a trace of nitrogen in silicon oxide because of the presence of nitrogen adsorbed on the walls of processing chambers and containers or which was present on the surface of the substrate before formation of the silicon oxide dielectric layer. Thus it is believed to be manifest that the mention of the phrase "substantially void of nitrogen atoms" by Trivedi '395 was a defensive assertion intended to

**avoid the making an extreme and probably incorrect statement that the layer 32 is totally devoid of nitrogen, which would be a physically impractical objective because of the ubiquity of nitrogen in the environment surrounding the workpieces prior to processing and adsorbed in the hardware and materials employed in processing. Accordingly, what Trivedi '395 teaches is the opposite of teaching that the layer 32 contains nitrogen, but it teaches that it is intended that almost no nitrogen should be present. There is not teaching of providing an optimum level of nitridization of the dielectric layer 32.**

**Further support for the above argument is found in the Summary of the Invention, Col. 2, lines 14-54, of Trivedi '395 states as follows:**

"In accordance with an aspect of the invention, a semiconductor processing method of forming field effect transistors includes forming a first gate dielectric layer over first and second areas of a semiconductor substrate. The first area is configured for forming p-type field effect transistors and the second area is configured for forming n-type field effect transistors. **The first gate dielectric layer includes silicon dioxide having nitrogen atoms concentrated therein**, the nitrogen atoms being higher in concentration within the first gate dielectric layer at one elevational location as compared to another elevational location. The nitrogen concentration at the one elevational location preferably ranges from 0.1% molar to 10.0% molar. The first gate dielectric layer is removed from over the second area while leaving the first gate dielectric layer over the first area. After removing the first gate dielectric, a second gate dielectric layer is formed over the second area. **The second gate dielectric layer includes silicon dioxide** proximate an interface of the second gate dielectric layer with the semiconductor substrate and the **second gate dielectric layer is substantially void of nitrogen atoms.** Next, transistor gates are formed over the first and second gate dielectric layers, and then p-type source/drain regions are formed proximate the transistor gates in the first area and n-type source/drain regions are formed proximate the transistor gates in the second area."

"In another aspect of the invention, integrated circuitry includes a semiconductor substrate having an area within which a plurality of n-type and p-type field effect transistors are formed. The respective transistors include a gate, a first gate dielectric layer for the p-type transistors and a second gate dielectric layer for the n-type transistors, and source/drain regions. **The first gate dielectric layer includes silicon dioxide having nitrogen atoms therein**. The nitrogen atoms are higher in concentration within the first gate dielectric

> layer at one elevational location as compared to another elevational location. The nitrogen concentration preferably ranges from 0.1% molar to 10.0% molar. **The second gate dielectric layer includes silicon dioxide material proximate an interface of the second gate dielectric layer with the semiconductor substrate which is substantially void of nitrogen atoms.** [*Emphasis added. It is noted that the line numbers do not line up properly in the patent in Col. 2.*]

**It is respectfully submitted that Trivedi '395 does not suggest tuning of different optimized levels of nitridization in NFET and PFET devices. The summary of the invention of Trivedi '395 teaches adding nitrogen to the first gate dielectric layer of the one gate dielectric and forming the second gate dielectric layer, with only a possible inadvertent trace of nitrogen being present in the second gate dielectric layer. Since Col. 2 is the summary of the invention, there is no mention of reference numeral "28" or reference numeral "32" in Col. 2. There is only a teaching of extreme differences in nitridation from a substantial degree in one case as contrasted with substantially void in the other case. That is nothing like "optimized" levels of nitridation. It is believed to be clear that the word "substantial" was employed in Trivedi '395 to cover the possibility that unwanted traces of nitrogen might be present in layer "32" due to contamination with nitrogen which is adsorbed in the processing equipment or nitrogen contamination which was present on the surface of the device prior to processing.**

**It is clear that the first gate dielectric layer 28 is intended to have nitrogen atoms therein, as described at Col. 4, lines 10-33 of Trivedi '395, which reads as follows:**

> Referring to FIG. 3, an interface 31 is indicated where first gate dielectric layer 28 meets substrate material 16/18. **First gate dielectric layer 28 is formed to have nitrogen atoms therein**, the nitrogen atoms being higher in concentration within the first dielectric layer at one elevational location as compared to another elevational location. The nitrogen concentration could peak at any elevational location, preferably in a region 30 at a location proximate interface 31. Further preferably, the nitrogen atoms are provided to have a concentration of from 0.1% molar to 10.0% molar within region 30, and more preferably from 0.5% to 5.0% molar. An exemplary thickness for region 30 is from 30 to 60 angstroms. Processing to produce the FIG. 3 construction could be conducted in a number of different manners. For example, the semiconductor substrate 10 can be provided in a furnace

(not shown) for thermal processing. An example processing is at a temperature ranging from 750° to 950°C., ideally 850°C., and at atmospheric pressure. A nitrogen source 50 is provided at about 100 to 10,000 sccm, ideally 1,000 sccm, for a period of from 5 minutes to 2 hours, ideally 30 minutes. The preferred sources of nitrogen have an N----O bond because of the ease of breaking the nitrogen bonds. However, other sources can be used. Examples include, in descending order of preference: NO, $N_2O$, $NH_3$ and $N_2$.

**Referring to Col. 5, lines 9-38 of Trivedi '395 , it is clear that the second gate dielectric layer 32 is intended to be composed of silicon oxide with substantially no nitrogen atoms therein.**

Referring to FIG. 5, a second gate dielectric layer 32 is primarily formed over the other of the first and second areas 12/14. Preferably, a second gate dielectric layer 32 is formed in the same manner as previously described above for first gate dielectric layer 28 (excluding the process forming the nitrogen region 30). Accordingly, **second gate dielectric layer 32 is preferably formed to comprise an oxide, such as silicon dioxide**, proximate interface 31 of second gate dielectric layer 32 with semiconductor substrate material 16. Alternative methods to form second gate dielectric layer 32 include performing one or any combination of the previously described "dry" and "wet" methods for forming first dielectric layer 28.

"As illustrated, the process to form second gate dielectric layer 32 preferably provides the primary layer for second gate dielectric over the n-type region 14. The thickness of second gate dielectric layer 32 can be selected or optimized for the second area 14 transistors by varying process conditions, such as temperature, pressure and processing time. Additionally, as indicated, the process can result in an additional layer over first gate dielectric layer 28, preferably less than 5 angstroms. Accordingly, first area 12 transistors and second area 14 transistors can have their gate dielectric properties separately and selectively optimized. **Further, most preferably, second gate dielectric layer 32 is fabricated to be substantially void of nitrogen atoms unlike the fabrication of first gate dielectric layer 28 proximate interface 31. In the context of this document, "substantially void of nitrogen atoms" means any nitrogen atom concentration less than or equal to 0.1% molar.**

USPTO RELIANCE ON COMMON SENSE AND BASIC KNOWLEDGE

It is possible that the Office Action may contain an allegation based on Official Knowledge where the Office Action stated as follows"

> "Therefore nitridation occurring in some form on NFET gate dielectric is at least suggested in Trivedi et al. Trivedi et al. also disclose that nitrogen concentration in PFET gate dielectric and in NFET gate dielectric are different and nitrogen concentration in PFET gate oxide layer is higher than that of NFET gate oxide layer."
>
> "It would have been obvious to one having an ordinary skill in the art at the time the invention was made to incorporate teachings of Trivedi et al. in forming a semiconductor device with NFET and PFET devices with the object of optimizing the electrical properties of thin gate dielectrics of PFET and NFET devices."

Thus the Examiner is challenged to provide evidence to support those allegations which are not believed to be supported by the teachings in the Trivedi '395. *In re Zurko*, 258 F.3d 1379, 59 U.S.P.Q.2d 1693 (Fed. Cir. 2001), "the Board cannot simply reach conclusions based on its own understanding or experience — or on its assessment of what would be basic knowledge or common sense. Rather, the Board must point to some concrete evidence in the record in support of these findings" (emphasis added).

The Office Action stated further as follows:

> "Claims 2, 4, 6, 8, 11, 13, 14, 16, 17, 18 and 19 are objected to as being dependent upon a base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims."
>
> "The primary reason :For the indication of allowability of Claims 2,4,6, 8, 11, 13, 14, 16, 17, 18 and 19 is the inclusion therein, in combination as currently claimed, of the limitation of a method of forming CMOS semiconductor materials with PFET area and NFET area comprising capacitor wherein the properties of the gate dielectric are tuned with different levels of nitridation of the gate dielectric."

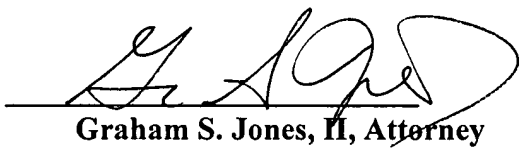
The above claims 2, 4, 6, 8, 11, 13, 14, 16, 17, 18 and 19 and the parent claims upon which they are dependent are now believed to allowable in view of the amendments to the claims and the above remarks.

A fee of $110.00 for the Petition for Extension of time of one (1) month which is being paid for by the enclosed Credit Card Payment Form PTO-2038 with a Fee Transmittal for FY 2004 PTO/SB/17 attached thereto.

No additional fee is believed to be due for the submission of this amendment aside from the If any additional fees are required, please charge any other such fees to Deposit Account No. 09-0458 as authorized in the additional Fee Transmittal for FY 2004 PTO/SB/17.

In view of the amendments and the above remarks favorable action including allowance of the claims and the application as a whole are respectfully solicited.

Respectfully submitted,

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